TRANSCEIVER DEVICE WITH A TRANSMIT CLOCK SIGNAL PHASE THAT IS PHASE-LOCKED WITH A RECEIVER CLOCK SIGNAL PHASE

ABSTRACT OF THE DISCLOSURE

A transceiver system is disclosed that includes a plurality of transceiver chips. Each transceiver chip includes one or more SERDES cores. Each SERDES core includes one or more SERDES lanes. Each SERDES lane includes a receive channel and a transmit channel. The transmit channel of each SERDES lane is phase-locked with a corresponding receive channel. The transceiver system has the capability of phase-locking a transmit clock signal phase of a transmitting component with a receive clock signal phase of a receiving component that is a part of a different SERDES lane, a different SERDES core, a different substrate, or even a different board. Each SERDES core receives and transmits data to and from external components connected to the SERDES core, such as hard disk drives. A method of transferring data from a first external component coupled to a receive channel to a second external component coupled to a transmit channel is also disclosed.